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PRELIMINARY AMENDMENT

Inventor(s): Kenichi Kawaguchi et al.

Title: PROCESSOR FOR MAKING MORE EFFICIENT USE OF
IDLING COMPONENTS AND PROGRAM CONVERSION
APPARATUS FOR THE SAME

Attorney's
Docket No.: NAK1-BG45a

EXPRESS MAIL LABEL NO. EL852658673US

DATE OF DEPOSIT: March 14, 2001

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Kenichi Kawaguchi

Serial No.:

Filed:

For: PROCESSOR FOR MAKING MORE
EFFICIENT USE OF IDLING COMPONENTS
AND PROGRAM CONVERSION
APPARATUS FOR THE SAME

Previous Examiner: S. Whitmore

Previous Group Art Unit: 2784

Irvine, CA 92614

March 14, 2001

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Prior to an examination on the merits of the above-identified application, please enter the following amendments:

IN THE SPECIFICATION:

Page 1, after line 7, insert:

Related Applications

This application is a divisional application of U.S. Serial No. 09/280,363 filed on March 29, 1999.

IN THE CLAIMS:

Please cancel Claims 1-17 without prejudice.

Please add the following newly-drafted Claims 21-23.

1 21. A program conversion apparatus that changes a source program to an object
2 program for a target processor executing long-word instructions, comprising:

3 a retrieving unit, for retrieving a pair of instructions from the source program, the
4 pair of instructions comprising a first instruction denoting a first calculation of two variables
5 and a second instruction indicating a second calculation, different than the first calculation,
6 of the same two variables;

7 a generating unit, for generating a special instruction corresponding to the retrieval
8 pair of instructions, the special instruction comprising an operation code denoting the first
9 calculation and the second calculation, and two operands representing the two variables; and

10 an arranging unit, for arranging the generated special instruction into a long-word
11 instruction.

1 22. The program conversion apparatus of Claim 21, wherein the first instruction denotes
2 addition, and the second instruction denotes subtraction.

1 23. The program conversion apparatus of Claim 22, wherein:

2 the target processor includes a first instruction execution unit having a first
3 calculation unit, and a second instruction execution unit having a second calculation unit and
4 a multiplication unit; and

5 the arranging unit retrieves a multiply instruction that does not share dependency
6 with the special instruction generated by the generating unit, and arranges the special
7 instruction and the multiply instruction into one long-word instruction.

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REMARKS

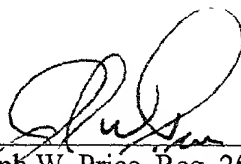
The newly-drafted claims provide an alternative definition of the invention and are within the scope of the original application.

This is a divisional application of U.S. Serial No. 09/280,363. It is requested that the references cited in the prosecution of the parent application be considered in the prosecution of this divisional application, and accordingly these references are cited on the attached form PTO 1449. The relevance of those references was set forth in the prosecution of U.S. Serial No. 09/280,363.

If the Examiner believes that a telephone interview will help further the prosecution of this case, he is respectfully requested to contact the undersigned attorney at the listed telephone number.

Very truly yours,

PRICE AND GESS



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I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to the Assistant Commissioner for Patents, Washington DC 20231

on

March 14, 2001



Signature

March 14, 2001

Date

VERSION WITH MARKINGS TO SHOW CHANGES MADE

A paragraph has been added before the paragraph beginning on page 1, line 8.

Claims 21-23 have been added.

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